ABSTRACT

[102] Aspects of the invention include a 3:2 pull down detector coupled to a 3:2 cadence processor and a color edge detector coupled to a binder. The binder may be coupled to a 3:2 cadence processor. A filter, which may be a temporal or infinite impulse response filter, may be coupled to the binder. A selector may also be coupled to the 3:2 cadence processor. A memory and a processor may also be coupled to any of the 3:2 pull down detector, the 3:2 cadence processor, the color edge detector, the binder, the filter and said output selector. The selector may select between a filtered deinterlaced output and a reverse 3:2 pull down output.